A Bidirectional High-frequency Link Inverter Using Center-tapped Transformer

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Abstract—**In this paper, a bidirectional high-frequency link inverter is proposed. The main feature of the inverter is that the electrical isolation is provided by a high-frequency center-tapped transformer. Furthermore, the sinusoidal Pulse Width Modulation method is modified so that the transformer can be utilized near to its full potential. As a result, the power switches count is reduced, and the efficiency increased. A 1kW prototype inverter is built and typical results are presented.**

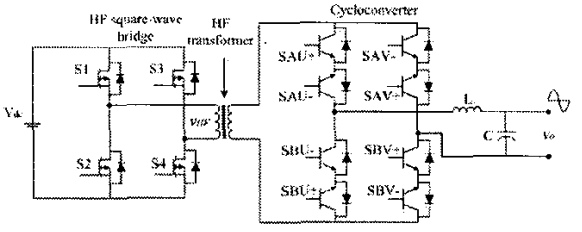
Keywords—**Bidirectional, HF transformer, Inverter, Pulse width modulation.**

I. INTRODUCTION

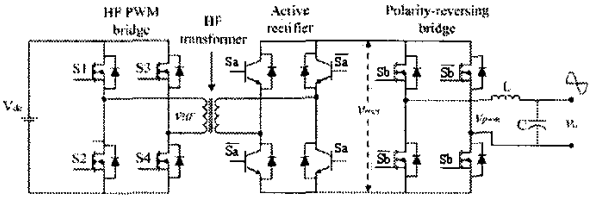
The merits of high-frequency (HF) link inverter are widely recognized, and its application has covered areas such as Uninterruptible Power Supply (UPS) and renewable energy source systems. Compared to the conventional Pulse Width Modulation (PWM) inverter, the HF link inverter offers significant reduction in size and weight due to the absence of line-frequency (50Hz) transformer. The two well-known HF link inverters are the "cycloconverter" [1] and the "dc-dc converter" [2] types, shown in Fig. 1 (a) and 1 (b) respectively. Both inverters are capable to perform bidirectional power flow, where the reactive power can be transferred back to the dc source.

The cycloconverter type consists of two power conversion stages, namely the HF square-wave bridge and the cycloconverter. For a single phase output, the total switches are twelve. At the HF square-wave bridge, the four switches are switched to construct a HF square-wave voltage with an approximately 50% duty cycle. At the cycloconverter stage, the sinusoidal output voltage is obtained by chopping the HF square-wave. The disadvantage of this topology is that all the power switches are operated at high frequency, resulting in relatively high switching losses. Furthermore, the switching scheme at the cycloconverter stage is complex.

The dc-dc converter type consists of three power stages, i.e. HF PWM bridge, active rectifier and polarity-reversing bridge. This topology also consists of twelve switches, but the unfolding stage (polarity-reversing bridge) is operated at line-frequency. Therefore, the switching losses are reduced. However, as the HF PWM bridge is PWM modulated, the HF transformer is less efficient compared to the cycloconverter type.



(a) Cycloconverter type HF link inverter.



(b) Dc-dc converter type HF link inverter.

Fig. 1. Bidirectional HF link inverters.

In this paper, we propose an alternative topology, which overcomes some of the abovementioned disadvantages. The proposed topology is similar to the dc-dc converter type, with two modifications:

1) implementing a modified modulation technique for the HF PWM bridge stage,
2) replacing the full bridge active rectifier with a center-tapped active rectifier.

The proposed topology reduced the number of power switches, and expectedly an increase in the efficiency. Besides, the modified PWM technique allows the transformer utilization near to its full potential.

II. CIRCUIT DESCRIPTION

A. Operation Principles

The proposed circuit configuration is shown in Fig. 2. There are basically three conversion stages: HF PWM bridge, active rectifier and polarity-reversing bridge.

At the first stage, the HF PWM bridge converts the dc voltage into HF PWM voltage, v_{HF}. Then, the power is transferred to the second stage through the HF center-tapped transformer. At this stage, the HF PWM voltage will be

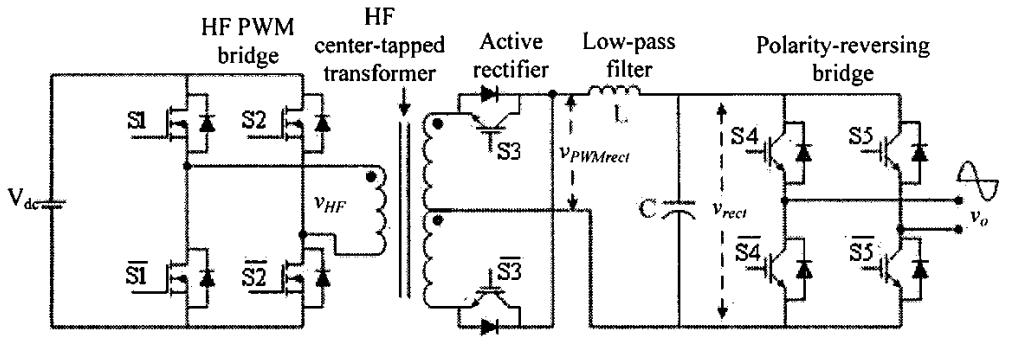


Fig. 2. The proposed bidirectional HF link inverter.

rectified using a center-tapped active rectifier. The active rectifier enables bidirectional power flow in the case of inductive load. If the power is transferred from the source to the load, the diodes are utilized. If the power flows in the reverse direction, power switches S3 and $\overline{S3}$ are turned-on. It must also be noted that every switch of the active rectifier requires a snubber to reduce high voltage spike that results from the leakage inductance of the transformer secondary. The snubber circuit is not shown in the block diagram for simplicity. The rectified PWM voltage, $v_{PWMrect}$, is then low-pass filtered to remove the high order harmonics and the rectified sinusoidal voltage, v_{rect} is obtained. Finally, using a polarity-reversing bridge, the second half of the rectified sinusoidal voltage waveform is inverted at zero-crossing, producing the sinusoidal output voltage, v_o. Note that the polarity-reversing bridge is only operated at line-frequency (50Hz). The timing diagram of the key waveforms is illustrated in Fig. 3.

Fig. 4 shows the timing diagram of the gate control signals for the conversion stages. The PWM control signal for the HF PWM bridge, v_{pwm}, is produced by comparing a rectified sinusoidal modulating signal with a triangular carrier signal. The control signal, v_s is used to control the power flow at the active rectifier stage. Note that the frequency of v_s is half of v_{pwm}. The control signal for polarity-reversing bridge is denoted as v_u.

Using this configuration, the total number of power switches is reduced into ten. From these, only six switches are switched at high frequency.

B. *Modulation Technique*

In this work, the PWM scheme of the HF PWM bridge is based on symmetrical regular sampling technique. The derivation of the switching angles is accomplished using the volt-second equalization method [3], as depicted in Fig. 5. The equation used to calculate the pulse width of the kth pulse for a given modulation index, M_I, and modulation ratio, m_f, is as follows:

$$\delta_k = 2\delta_o M_I \sin\alpha_k \qquad (1)$$

where $k = 1 \ldots \left(\frac{m_f}{2}\right)$.

Using (1), the switching angle, i.e. the rising and falling edges of kth pulse can be calculated:

$$\text{Rising edge, } \alpha_{1k} = \alpha_k - \frac{\delta_k}{2} \qquad (2)$$

$$\text{Falling edge, } \alpha_{2k} = \alpha_k + \frac{\delta_k}{2} \qquad (3)$$

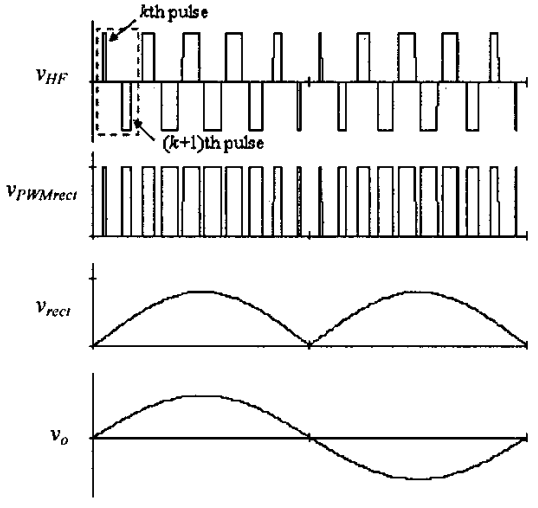


Fig. 3. Key waveforms at the principal conversion stages.

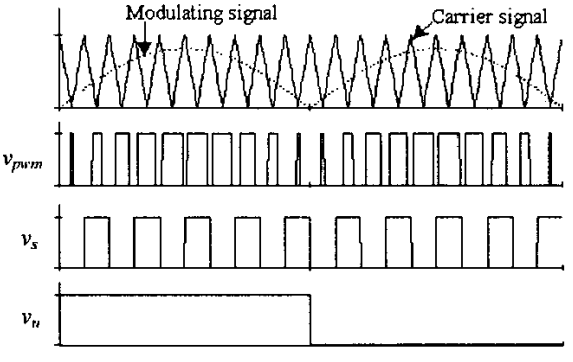


Fig. 4. Gate control signals at the principal conversion stages.

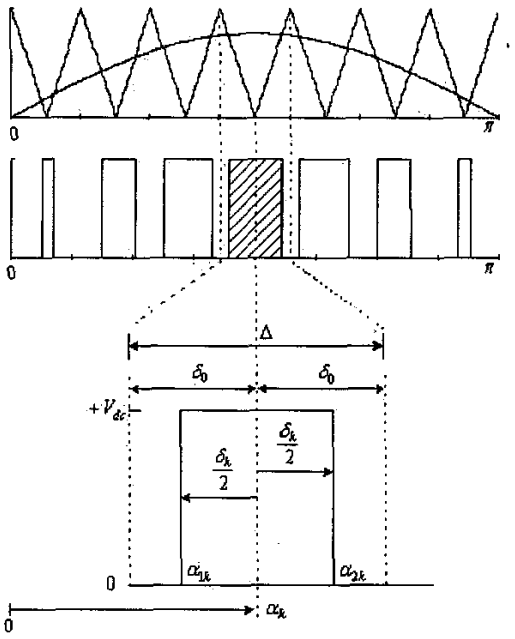


Fig. 5. Volt-second modulation method.

From Fig. 3, it can be noticed that the pulse width for kth and $(k+1)$th pulses are not equal in v_{HF}. If the difference in the pulse widths are plotted from $k = 1$ through m_f, it can be observed that a low frequency voltage envelope exists along with the high frequency component. This may lead to possible transformer saturation, as the transformer is designed for high frequency operation.

To overcome this problem, a modified PWM technique is proposed, where the pulse width of the kth pulse is equalized to the $(k+1)$th pulse, as shown in Fig. 6. Using this approach, the use of dc blocking capacitance at primary side of transformer [2] is avoided. Furthermore, the processing speed to calculate the pulse widths can be increased, with only $m_f / 8$ pulses to be calculated in each sinusoidal cycle. The pulse widths are calculated using the following equation:

$$\delta_k = \delta_{(k+1)} = 2\delta_o M_I \sin(\alpha_k') \qquad (4)$$

where:

$$\alpha_k' = \frac{\alpha_k + \alpha_{k+1}}{2}, k = 1,3,5..\left(\frac{m_f}{2} - 1\right).$$

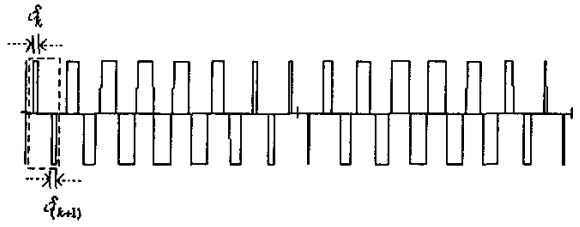


Fig. 6. The equalized pulse pairs.

C. Dead-time Compensation

The dead-time compensation utilized the pulse-based dead-time compensator (PBDTC) method [4]. This approach compensates the dead-time on pulse-by-pulse basis, where the lost volt-second is added back in each pulse. From Fig. 7 (a), it can be seen that an amount of dead-time, t_d ,is lost from the pulse width of $v_{PWMrect}$. Based on the PBDTC method, the amount of dead-time lost is added at the positive edge of v_{PWM} pulse, as shown in Fig. 7 (b). The added portion will be subtracted by the dead-time generator. As a result, the actual pulse is identical to the ideal pulse.

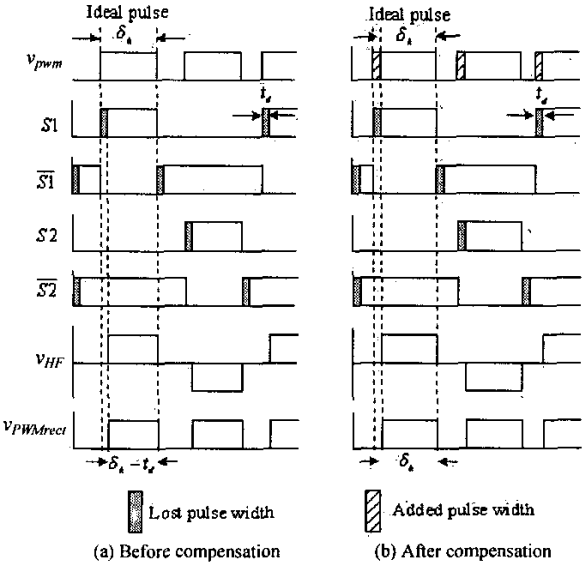


Fig. 7. Dead-time compensation scheme for the HF PWM bridge.

III. IMPLEMENTATION AND EXPERIMENTAL RESULTS

To validate the viability of proposed topology, a 1kW prototype is designed and built. Fig. 8 shows the photograph of the constructed prototype. The HF PWM bridge is built using the IRFP460 power MOSFET. The power transformer is wound on the ETD59 ferrite core. The active rectifier is built using the IRG4PH40K IGBT and 20EFT10 fast recovery diode, with rated voltage at 1200 V. In addition, the *RC* snubber circuit has been placed at every switch to reduce the surge voltage. The polarity-reversing bridge is constructed using SK25GB065 IGBT module. Since almost all the surge voltages have been filtered before entering polarity-reversing bridge, the chosen rated voltage for the power switches is only 600V.

All the power switches are driven by a Hewlett Packard gate driver chip, HCPL3120. This chip has a built-in opto-coupler, mid-stage amplifier and output-stage (power) amplifier. The "all-in-one-chip" solution has greatly simplified the interfacing process. To obtain isolated power supplies for the bridge leg, each driver is equipped with

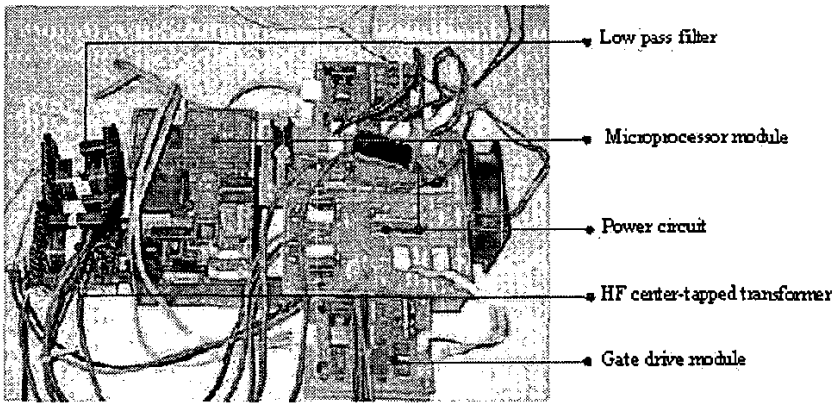


Fig. 8. Photograph of the prototype inverter.

transformer isolated dc-dc converter, supplied from a single 9V battery. The isolated dc-dc converter is driven by the SG3524 pulse generator and isolation is performed by the ET12 Ferro-cube high frequency miniature transformer.

Siemens SAK-C167CS-LM (16 bit fixed-point microcontroller) has been chosen to generate PWM signals for the HF PWM bridge. It is also used to generate the gate signals for the active rectifier, v_s, and the polarity-reversing bridge, v_u. The signals generated will then go through a series of external logic gates, as shown in Fig. 9, and become the input signals of gate drives.

Laboratory experiments have been carried out, with the following specifications:

- Input voltage ranged from 130V to 150V.
- Sinusoidal output voltage 220-250V_{rms}, 50Hz.
- Maximum output power of 1kW.

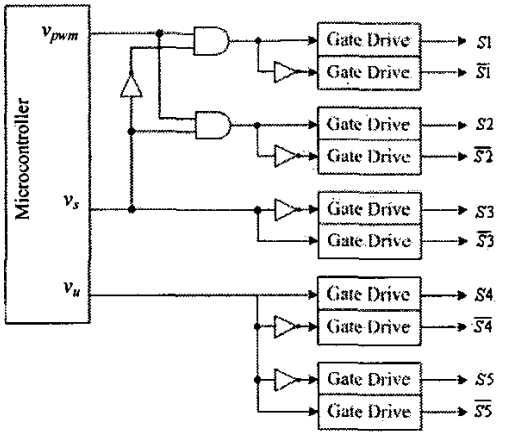
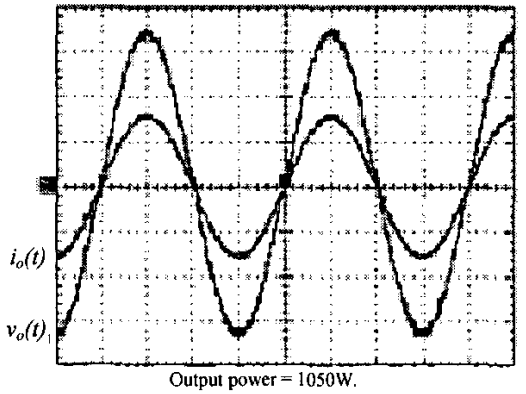


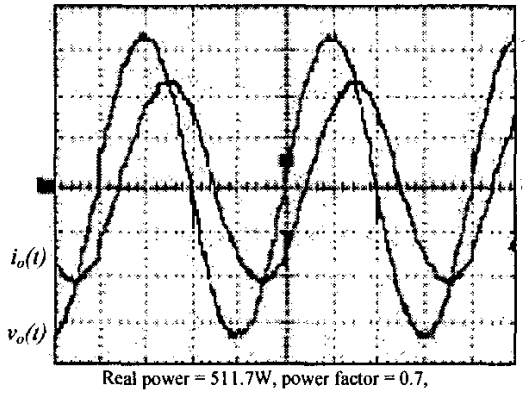
Fig. 9. Interface between the microcontroller with the power switches.

Fig. 10 and Fig. 11 show the experimental results for resistive and inductive load respectively. From Fig. 11, it can be noted that the inverter is capable of carrying bidirectional power flow.



Output power = 1050W.
Scales: output voltage 100V/div, output current 4A/div, time 5ms/div.

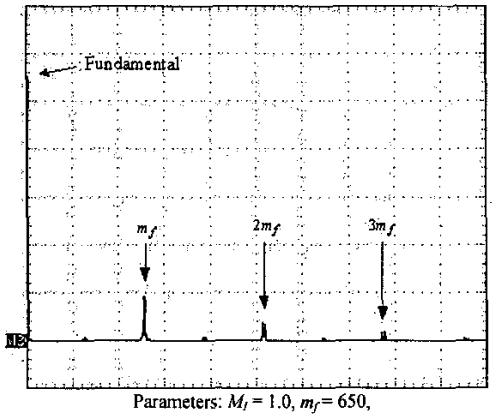
Fig. 10. Output voltage and current with resistive load.



Real power = 511.7W, power factor = 0.7,
Scales: output voltage 100V/div, output current 2A/div, time 5ms/div.

Fig. 11. Output voltage and current with inductive load.

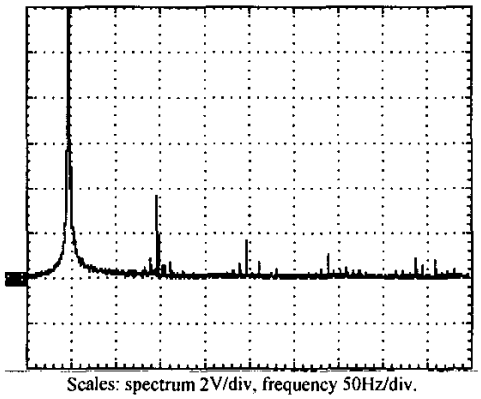
The harmonics of the inverter output can be measured by disconnecting the *LC* low pass filter from the inverter. The measured frequency spectrum measured is shown in Fig. 12. It can be seen that the main harmonic components exist at the multiples of fundamental switching frequency, which are m_f, $2m_f$, $3m_f$ and $4m_f$. Owing to the pulse pairs equalization, there are sub-harmonics exist at $0.5m_f$, $1.5m_f$ and $2.5m_f$. However, the magnitudes of the sub-harmonics are very small and negligible.



Parameters: M_f = 1.0, m_f = 650,
Scales: spectrum 40V/div, frequency 12.5kHz/div.

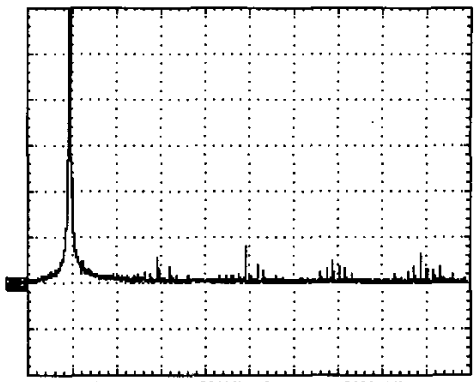
Fig. 12. Frequency spectrum of the output voltage without *LC* filter.

Fig. 13 (a) and 13 (b) shows the frequency spectrum of the filtered output voltage before and after dead-time compensation, respectively. The dead-time to pulse period ratio (t_d / T_s) is set to 0.1. As can be seen, most of the low order harmonics (3rd, 5th, etc) result from the dead-time effect is reduced. Fig. 14 indicates the efficiency of the dead-time compensation technique. Even as t_d / T_s is increased to a large value, i.e. 0.25, the compensation scheme still works well.



Scales: spectrum 2V/div, frequency 50Hz/div.

(a) Frequency spectrum before dead-time compensation.



Scales: spectrum 2V/div, frequency 50Hz/div.

(b) Frequency spectrum after dead-time compensation.

Fig. 13. Frequency spectrum of the filtered output voltage before and after dead-time compensation.

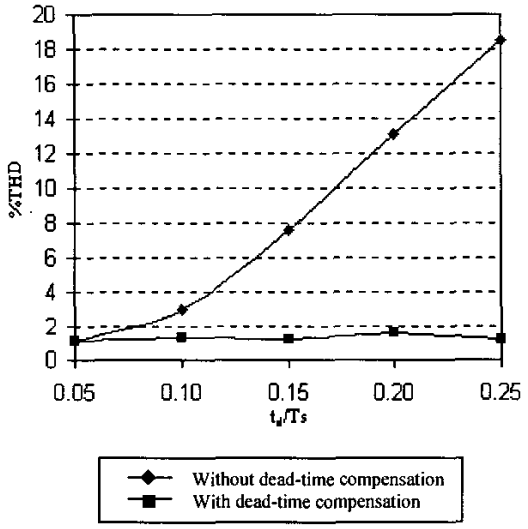


Fig. 14. Efficiency of dead-time compensation for various values of t_d / T_s.

Fig. 15 shows the measured efficiency of the inverter at principal conversion stages. The average efficiency of the HF PWM bridge is 95%, while the average efficiency of the HF center-tapped transformer is 91%. Taken as a whole, the average total efficiency of the system is 88%. Note that when the output power increases to 1kW, the average efficiency decreases to the minimum level of 87%. This can be attributed to the increased losses of power switches and transformer at high current operation.

The measured output voltage THD for resistive load is shown in Fig. 16. It can be seen that the output voltage THD is less than 1% over the entire output power, with the average value of approximately 0.5%. The average value is far less than 5%, the industrial standard for UPS systems. The minimum value of THD (0.35%) is obtained when the inverter is operated at output power 600-700W.

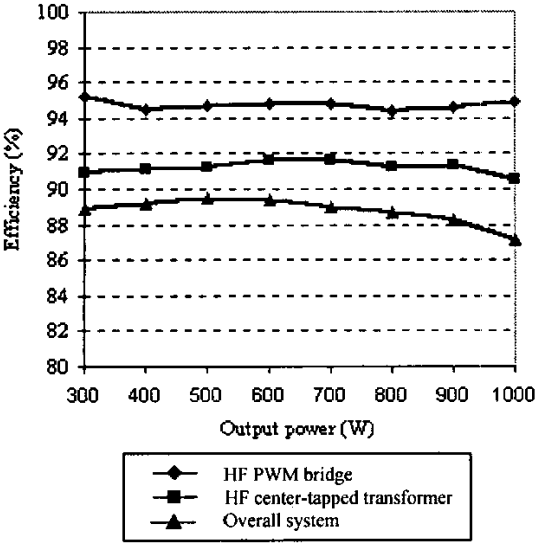


Fig. 15. Efficiency against output power at the principal stages of the inverter.

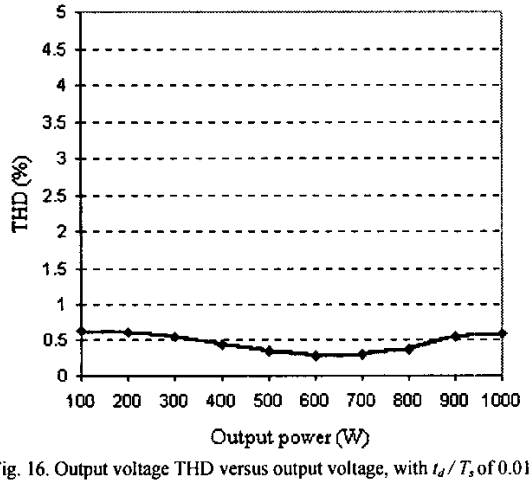


Fig. 16. Output voltage THD versus output voltage, with t_d / T_s of 0.01.

IV. CONCLUSION

A bidirectional HF link inverter using center-tapped transformer has been described. Using this topology, the number of power switches is reduced, thus increasing the overall system efficiency. The modified digital PWM technique allows better utilization of the HF transformer and increases the calculation processing speed. A 1kW prototype has been constructed to verify the proposed topology. Experimental results show that the output voltage has very low THD (<1%), with average overall efficiency of 88%. The proposed inverter is suitable for application in UPS or renewable energy source systems.

ACKNOWLEDGMENT

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